CLAIMS

1 A power semiconductor device comprising a two-dimensional array of individual cells formed on a semiconductor substrate (62), each individual cell having source regions (37) within base regions (36) in the semiconductor substrate (62),
characterised in that the source regions (37) of the individual cells of the array comprise a plurality of source region branches (80) each extending radially towards at least one source region branch of an adjacent cell, the source region branches of adjacent cells presenting juxtaposed ends, the base regions (36) of the individual cells of the array comprising a corresponding plurality of base region branches (80) extending radially towards at least one base region branch of an adjacent cell, and the base region branches (80) of adjacent cells merging together adjacent and between said juxtaposed ends to form a single and substantially uniformly doped base region (36) surrounding said source regions (37) of the individual cells of said array.

2 The power semiconductor device according to claim 1 wherein said plurality of radially extending branches (80) of an individual cell intersect at a central enlarged area (48) having contact cut-out portions (41) whose width (43) is larger than the width (44) of said radially extending branches.

3 The power semiconductor device according to claim 2 wherein the cut-out (41) portions of said enlarged area (48) are straight segments or concave curves with an inverse curvature radius.

4 The power semiconductor device according to any one of the previous claims wherein said radially extending branches (80) of each individual cell are linear or non-linear, with constant width or variable width.

5 The power semiconductor device according to any one of the previous claims wherein each individual cell has at least three radially extending branches arranged in such a way that the area defined by the merging adjacent branches is a polygon.

6 The power semiconductor device according to any preceding claim and comprising at least one drain electrode (83) contacting a face of said semiconductor substrate (62) opposite said source regions (37).

7 The power semiconductor device according to any of claims 1 to 5 further comprising physically isolated drain regions (39) in the substrate (62) and wherein said physically isolated drain regions (39) have a depth (69) equivalent to the depth of said base regions (36).

8 The power semiconductor device according to claim 7 wherein said individual cells forming a plurality of source regions (37, 48) and separating said physically isolated drain regions (39) are packed into a relatively small area to contain at least 10 physically isolated drain regions (39).

9 The power semiconductor device according to any preceding claim wherein said cells of said array form field effect transistors.

10 A method for manufacturing a power semiconductor device comprising the steps of:
forming a two-dimensional array of individual cells on a semiconductor substrate (62), each individual cell having source regions (37) within base regions (36) in the semiconductor substrate (62),
characterised in that the source regions (37) of the individual cells of the array comprise a plurality of source region branches (80) each extending towards at least one source region branch of an adjacent cell, the source region branches of adjacent cells presenting juxtaposed ends,

the base regions (36) of the individual cells of the array comprising a corresponding plurality of base region branches (80) extending radially towards at least one base region branch of an adjacent cell, and the base region branches (80) of adjacent cells merging together adjacent and between juxtaposed ends to form a single and substantially uniformly doped base region (36) surrounding said source regions (37) of the individual cells of said array.

11 A method for manufacturing a power semiconductor device as claimed in claim 10 comprising the steps of:

- forming said base regions (36) extending from a first surface (92) of said semiconductor substrate (62) with radially extending base region branches (80);
- forming said source region (37) within each base region (36) of each individual cell with said radially extending source region branches (80);
- forming a gate oxide region (76) over said first surface (92);
- forming a source electrode (82) in contact with said source regions (37) of each individual cell within each of the plurality of the base regions (36); and
- forming a drain electrode (83) in contact with a second surface (94) of said semiconductor substrate (62) opposite to said first surface (92).

12 A method for manufacturing a power semiconductor device as claimed in claim 10 comprising the step of forming in said first surface (92) physically isolated drain surface regions (39) surrounded by said plurality of base regions (36).

13 The method of manufacturing a power semiconductor device according to any of claims 10 to 12 wherein forming said base regions comprises the step of merging said base regions (36) of each individual cell so as to form a single base region (36).

14 The method of manufacturing a power semiconductor device according to any of claims 10 to 13 wherein forming said base regions comprises the step of making ion implant of high voltage breakdown resistance for the base regions (36) before forming a source electrode (82) over said first surface.